Supreme Court, U.S.
FILED
AUG 10 1988
JOSEPH F. SPANIOL, JR.
CLERK

No. 88-308

IN THE

SUPREME COURT OF THE UNITED STATES

TERM 1988 - 1989

JAMES N. CONSTANT,

Petitioner

v.

ADVANCED MICRO-DEVICES, INC., et al.,

Respondents *

APPENDIX B

PETITION FOR WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

James Constant
1603 Danbury Drive
Claremont, CA 91711
(714) 624-1801

Pro se petitioner

---

* see APPENDIX A for a complete list of all Respondents

APPENDIX B

Contents

Page

Judgment District Court B-2

Proposed Findings of Fact and

Consclusions of Law:

'635 Patent B-3

'491 Patent B-35

Order District Court Granting Costs

to Respondents B-65

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA
CASE NO. 85-0262-SVW
JUDGMENT
JAMES CONSTANT,
Plaintiff,
vs.
ADVANCED MICRO-DEVICES, INC., et al.,
Defendants.

The Court hereby enters judgment in accordance with the findings of facts and conclusions of law entered by the Court on October 28, 1987. Accordingly, the Court hereby enters its judgment finding invalid United States Patents numbered 3,950,635 and 4,438,491.

IT IS SO ENTERED.

DATED: November 6, 1987

STEPHEN V. WILSON

UNITED STATES DISTRICT JUDGE

Martin R. Horn
John Land
David A. Hall
SPENSLEY HORN JUBAS & LUBITZ
A Law Corporation
1880 Century Park East, Fifth Floor
Los Angeles, California 90067
(213) 553-5050
Attorneys for Defendant
HITACHI AMERICA, LTD.

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA
Civil Action No.CV 85-0262 SVW (Bx)
PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW RE: SUMMARY JUDGMENT OF INVALIDITY OF U.S. PATENT NO. 3,950,635.

JAMES CONSTANT,
Plaintiff,

v.

ADVANCED MICRO-DEVICES, INC., et al.,
Defendants.

Pursuant to this Court's Order at the May 4, 1987 hearing, defendant HITACHI AMERICA, LTD. ("HAL") submits the following proposed findings of fact and conclusions of law following this Court's granting of the HAL Motion for Summary Judgment of Invalidity of U.S.

Patent No. 3,950,635.

FINDINGS OF FACT

A. The Parties to the Motions and the Causes of Action

1. Plaintiff James Constant ("Constant") is an individual residing in Claremont, California. Constant has charged each of the defendants in this action with infringement of U.S. Patent No. 3,950,635 (the "'635 patent") and 4,438,491 (the "'491 patent).

2. This is a case of alleged patent infringement. All of the causes of action unrelated to patent infringement were dismissed with prejudice by order of the Honorable Pamela Ann Rymer on July 11, 1985.

3. Jurisdiction over defendants is predicated under the patent laws of the United States, 35 U.S.C. §§ 1, et

seq., pursuant to 28 U.S.C. § 1338 (a) and (b), and on other grounds related to the dismissed causes of action. (Complaint at paragraph 1).

4. Defendant HAL brought a motion for Summary Judgment of Invalidity of U.S. Patent No. 3,950,635. Defendant Intel brought a motion for Summary Judgment of Invalidity of the '491 patent.

5. Following a hearing and pursuant to agreement of the parties, this Court appointed Robert E. Hillman to act as a Special Master in this action pursuant to Rule 53 of the Federal Rules of Civil Procedure. (Order of Reference filed August 4, 1986).

6. Mr. Hillman is qualified to perform as a Special Master, having

practiced patent law for the last twenty-five years with extensive experience in patent prosecution and litigation, having an undergraduate degree from the Massachusetts Institute of Technology in physics and mathematics and a law degree from the Harvard Law School. (Defendant's Opposition to Plaintiff's Motion to Disqualify the Master and to Strike his Report to the Court at 4-5; letter from Paul S. Malingagio to Honorable Stephen V. Wilson dated July 31, 1986) (enclosing letter and resume from Robert E. Hillman).

7. Pursuant to the Order of Reference, the Special Master conducted hearings, reviewed submissions from the parties, and issued a "Report of Special Master on Validity of U.S.

Patent No. 3,950,635 and a Report of Special Master on Validity of U.S. Patent No. 4,438,491" (the "Master's Report"). (Transcript of Hearing before Special Master Hillman on September 4, 1986; Transcript of Hearing before Special Master Hillman on October 29, 1986; Order of Reference; Master's Report).

8. Following submission of the Master's Reports, Plaintiff filed a Motion to Disqualify the Special Master on various grounds. This Court held a hearing on March 16, 1987 on Plaintiff's Disqualification Motion. Having considered Plaintiff's arguments and evidence, the court denied Plaintiff's Disqualification Motion as being without factual basis.

9. This Court received the

Master's Reports and thereafter held hearings on March 30, 1987 and May 4, 1987. At these hearings, Constant had an opportunity to extensively examine the Special Master concerning the bases for the Special Master's recommendation. The Master's Reports are attached hereto as Exhibits A and B. This Court adopts the Master's Reports and independently makes these findings of fact and conclusions of law.

B. The '635 Patent - Findings of Fact

10. The '635 patent, titled "Digital Matched Filter and Correlator Using Random Access Memory," issued to James N. Constant on April 13, 1976 from application Serial No. 479,872 ("the '872 application") filed June 17, 1974. The '872 application was itself

a continuation-in-part of a subsequently abandoned earlier application, Serial No. 435,681 filed on January 23, 1974. Mr. Constant is the owner of the '635 patent and is the plaintiff in this action.

11. The Constant '635 patent describes and claims an invention relating to the digital implementation of "matched filters" and "correlators." Matched filters and correlators are used in a wide variety of electronic devices and perform a comparison of one electrical signal with a second electrical signal. One or both of the signals may be stored. (Appendix A of the Motion; Master's Report at 1).

12. More specifically, a "correlator"is a type of device in which the two electrical signals are

changing constantly, whereas a "matched filter" is a type of device in which one of the electrical signals is a fixed signal that is stored in the device memory. (Appendix A of the Motion; Master's Report at 1-3, 13; '635 patent at col. 7, lines 33-65).

13. The comparison of signals is implemented in the '635 patent by first representing the electrical signals as two sequences of digital values, respectively. The digital values are supplied to an exclusive-or gate that provides one binary output if the two digital values are the same and produces the opposite binary output if the two digital values are not the same. A sequence of pairs of digital values can be compared and the binary output of the exclusive-or gate can be

added together to give a number that indicates the overall degree of similarity between the two electrical signals. (Appendix A of the Motion; Master's Report at 1-3).

14. The Constant '635 device operates under control of a clock, which supplies regularly timed pulses to the various elements so that the electrical signal values will move to the exclusive-or gate at the proper time. An address counter is used to ensure that the proper electrical signal values are supplied to the gate. (Appendix B of the Motion; Master's Report at 5-6).

15. An address counter is required with the Constant device because the memory used for the electrical signals is a type of memory

called "random access memory" or "RAM" for short. Access to RAM cells is random in the sense that any desired memory cell can be accessed by appropriate setting of the address counter value. The memory cell can be accessed on any particular clock pulse. (Appendix B of the Motion; Master's Report at 6).

16. A shift register is a type of memory in which memory cell locations are lined up in single file and can be accessed only through the ends. No address counter is needed to control access to this type of memory. (Master's Report at 6-7).

17. In many signal processing applications using correlators or matched filters, the signals are stored in a "delay line" and then retrieved at

a rate greater than the rate of storage. This is often called time compression. A delay line is a data signal loop having a memory such that data is stored in the memory and released some time thereafter. One implementation of a delay line is the delay line time compressor (DELTIC), which recirculates signals in successive sampling intervals. ('635 patent at column 2, lines 21-29 and column 3, lines 48-57; Master's Report at 7-8 and 12-13).

18. The '635 patent contains fourteen claims. Claims 1 and 10 are independent claims directed to the digital implementation of matched filters and correlators. Claim 11 is an independent claim directed to a method for the digital implementation

of matched filters and correlators. The remaining claims are dependent claims.

19. Constant concedes that the only difference between the '635 patent and the prior art is the use of RAM, along with the required addressing circuitry, in place of shift register memory, in a correlator or matched filter. ('635 patent at column 2, lines 40-63; Master's Report at 7-8).

20. "Digital Compressed-Time Correlators and Matched Filters for Active Sonar" by W.B. Allen and E.C. Westerfield (the "Allen and Westerfield publication") was published in January of 1964 in the Journal of the Acoustical Society of America. (Exhibit L of Motion for Summary Judgment and Master's Report at 14).

21. The Allen and Westerfield publication describes delay line time compressors or DELTICs having either an acoustic or a shift register delay line and, as an alternative to either the acoustic or shift register delay line, the use of magnetic core memory in the delay line. The magnetic core memory delay line is illustrated in Figure 13 of the Allen and Westerfield publication and is referred to as a "MACOMATIC" or magnetic core matrix time compressor. (Exhibit L of Motion for Summary Judgment; Declaration of Professor Lawrence P. McNamee in Support of Motion (the "McNamee Declaration") at ¶¶9-11; Master's Report at 14-16).

22. Magnetic core memory is an early form of RAM that used magnetic

elements to store digital bits of data, rather than the semiconductor storage elements used in modern technology. Nevertheless, magnetic core memory is RAM; namely, it has the ability to access any memory cell location at random by simply addressing that cell directly. (McNamee Declaration at ¶8; Master's Report at 15).

23. The Allen and Westerfield publication fully discloses a matched filter or correlator using a random access memory. (McNamee Declaration at ¶¶9-11; Master's Report at 14-18, 24-29, 31-34).

24. U.S. Patent No. 3,295,107 for "Electronic Time Compression Device" issued on December 27, 1966 to Robert E. Stalcup (the "Stalcup patent"). (Exhibit K of the Motion for Summary

Judgment, Master's Report at 18).

25. The Stalcup patent fully discloses a matched filter or correlator using a random access memory for the delay line memory. (Stalcup patent at col. 1, line 70-col. 2, line 3; McNamee Declaration at ¶¶3-7; Master's Report at 18-24, , 29-34).

26. "High Speed Shift Registers Use TTL RAMs and Counters To Do All The Shifting by John Springer was published in Electronics Design on September 1, 1973 (the "Springer publication"). (Exhibit N of Motion for Summary Judgment; Master's Report at 13-14).

27. The Springer publication fully discloses in general the idea of using RAM in place of shift register memory. Springer does not explicitly apply that idea to matched filter or

correlators. (Exhibit N of Motion for Summary Judgment; McNamee Declaration at ¶14; Master's Report at 13-14).

28. The Springer publication was published prior to the date of conception of the device embodied in the '635 patent. Constant has admitted that the Springer publication taught him the use of RAM as a shift register and that Constant thereafter conceived of the device embodied in the '635 patent. (Deposition of James Constant conducted on March 20, 1986 at 79, line 23 to 80, line 2; Plaintiff's Objections to Master's Report-Part 2B, Exhibit 2; '635 Patent at column 4, lines 21-24; Master's Report at 13-14).

29. The Stalcup patent and the Allen and Westerfield publication disclose each and every element of

claims 1, 2, 6, 8, 9, and 11-14 of the '635 patent. The Allen and Westerfield publication in addition discloses each and every element of claim 7. (Master's Report at 24-30, 34-38). Constant's arguments with respect to the definition of RAM, the address "decoder," sequential addressing, clocking, shifting, and multiplying, are wholly lacking in any substance or support for the reasons set forth by the Master (id). These arguments do not raise any genuine issue of fact. (Master's Report at 24-30, 34-38).

30. Claim 1 of the '635 patent requires a first memory 1 and a second memory 11. Claim 1 requires the first memory to be RAM and allows the second memory to be any type of memory. Claim 2 requires that the second memory also

be RAM. The teachings of the Allen and Westerfield and Stalcup references are as exactly applicable to claim 2 as they are to claim 1, and therefore each of these references discloses each and every element of claim 2. (Motion at 16-18 and 47; Master's Report at 34).

31. The Allen and Westerfield publication and Stalcup patent both teach replacing shift registers with RAM in correlators and matched filters and the Springer publication teaches such a replacement generally. For the reasons set forth below, any one of these prior art references overwhelmingly, clearly and convincingly renders all claims of the '635 patent obvious. (Master's Report at 13-14, 31-38).

32. Constant has asserted that

the level of ordinary skill in the art would be an individual having a Ph.D. in electrical engineering or physics; this is undisputed. (Texas Instruments Memorandum of Points and Authorities in Support of Motion for Summary Judgment at 29; Deposition of James Constant conducted on March 20, 1986 at 118-19).

33. Claim 3 requires the second memory to be a read only memory and claim 4 requires the second memory to be a programmable read only memory, and claim 5 requires the second memory to be a bipolar signal generator. These are the only differences between those respective claims and the Stalcup and Allen and Westerfield references. ('635 patent).

34. It is uncontested that read only memory, programmable read only

memory and bipolar signal generators are alternative forms of random access memory and were so understood prior to Constant's claimed invention; Constant himself in the '635 patent acknowledges the equivalence between "a number of forms " of random access memory, including specifically DELTIC loop circuits, read only memory, programmable read only memory, and bipolar signals applied to a multiplier. ('635 patent, col. 4, lines 3-17; McNamee Declaration at ¶8; Master's Report at 35-36).

35. It would have been obvious for a person of ordinary skill in the art to substitute for the second memory a read only memory (claim 3), programmable read only memory (claim 4), or means for generating bipolar

signals (claim 5), as specified in the '635 patent, for the same reasons as claims 1 and 2, the additional elements of claims 3, 4, and 5 being equivalent to the elements of claims 1 and 2. (Motion at 16-18, 19-22, 47, 50-55; Master's Report at 35-36).

36. Claim 6 requires that the second memory be a DELTIC circuit; claim 8 requires that the first memory be a DELTIC circuit. These features are present in the Allen and Westerfield publication and also in the Stalcup patent, and therefore each of these references discloses each and every element of claims 6 and 8. ('635 patent; Master's Report at 36).

37. Claim 7 requires that the multiplier means of claim 1 be a set of multipliers, a feature present in

Figure 24 of the Allen and Westerfield publication. Thus, the Allen and Westerfield publication discloses each and every one of the elements of claim 7. ('635 patent; Master's Report at 37).

38. Claim 9 requires that the clock means of claim 1 includes a means for shifting the second signals in the second memory. This feature is disclosed by the Allen and Westerfield publication and by the Stalcup patent, so the each one of these references discloses each and every one of the elements of claim 9. ('635 patent; Master's Report at 37).

39. Claim 10 of the '635 patent discloses an admittedly prior art system using shift register memory, except that the first memory is

implemented as RAM rather than as a shift register. ('635 patent; Master's Report at 37).

40. It would have been obvious to one of ordinary skill in the art to substitute RAM for only one of the memories, just as well as substituting RAM for both of the memories, in view of the prior art references by either ALlen and Westerfield or by Stalcup. (Master's Report at 37).

41. Claim 11 of the '635 patent is a method claim which is the counterpart of the apparatus claim 1 and therefore each and every step of claim 11 is disclosed by each of the Allen and Westerfield or Stalcup references, which therefore anticipate claim 11. It also would have been obvious to one of ordinary skill in the

art to perform each and every one of the steps of claim 11 in view of either of those same references combined with the Springer publication. Such a combination is invited by Springer. (Master's Report at 38).

42. Claim 12 is a method claim which is the counterpart of claim 6, requiring the second memory to be a DELTIC circuit. Both the Allen and Westerfield and Stalcup prior art references disclose each and every one of the steps of claim 12. It also would have been obvious for one of ordinary skill in the art to perform each and every one of the steps of claim 12, in view of the same references combined with the Springer publication. (Master's Report at 38).

43. Claim 13 is a method claim

which is the counterpart of claim 8, requiring the first memory to be a DELTIC circuit. Both the Allen and Westerfield and Stalcup prior art references disclose each and every one of the steps of claim 13. It also would have been obvious to one of ordinary skill in the art to perform each and every one of the steps of claim 13, in view of the same references combined with the Springer publication. (Master's Report at 38).

44. Claim 14 is a method claim which is the counterpart of claim 9, requiring that the samples in the second memory be shifted as well as the samples in the first memory. Both the Allen and Westerfield and Stalcup prior art references disclose each and every one of the steps of claim 14. It also

would have been obvious to one of ordinary skill in the art to perform each and every one of the steps in claim 14, in view of the same references combined with the Springer publication. (Master's Report at 38).

C. The '635 Patent: CONCLUSIONS OF LAW

1. Jurisdiction is proper in this Court under 28 U.S.C. § 1338 (a) and (b).

2. Summary judgment is as appropriate in a patent case as in any other. Where no genuine issue of material fact remains and the moving party is entitled to judgment as a matter of law, courts should utilize Rule 56 of the Federal Rules of Civil procedure to avoid unnecessary expense to the parties and wasteful utilization

of the jury process and judicial resources. Barmag Barmer Maschinenfabrik AG v. Murata Machiner, Ltd., 731 F.2d 831, 835 (Fed. Cir. 1984).

3. With respect to whether there is a genuine issue of material fact, a court may not simply accept a party's statement that a fact is challenged. The party opposing a motion for summary judgment must point to an evidentiary conflict created on the record by at least a counter statement of facts set forth in detail by a knowledgeable affiant. Mere denials or conclusory statements are insufficient to create a genuine issue of material fact. Barmag, 731 F.2d at 836. Constant has presented no evidence at all of a genuine issue of material fact.

4. A statement by an applicant, whether in the application or in other papers submitted during prosecution of the application, that certain matter is "prior art" to the applicant is an admission that the matter is prior art for all purposes. In re Nomiya, 509 F.2d 566, 571 at n. 4 (C.C.P.A. 1975).

5. A patent is presumed valid under 35 U.S.C. § 282, and one attacking validity has the burden of proving invalidity by clear and convincing evidence. Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1375 (Fed. Cir. 1986).

6. A patent claim is anticipated under 35 U.S.C. § 102 is each element of the claim is found, either expressly described or under principles of inherency, in a single prior art

reference or if the claimed invention was previously known or embodied in a single prior art device or practice. That is, all the limitations of a claim must be found in a single reference. Kalman v. Kimberly Clark Corporation, 713 F.2d 760, 771 (Fed. Cir. 1983).

7. In determining obviousness under 35 U.S.C. § 103, the scope and content of the prior art are determined; differences between the prior art and the claims at issue are ascertained; and the level of ordinary skill in the pertinent art are resolved. Secondary considerations having a nexus to the claimed invention, such as commercial success, long felt but unsolved needs, and failure of others are to be utilized to give light to the circumstances

surrounding the origin of the subject matter sought to be patented and may have relevancy. Graham v. John Deere Company, 383 U.S. 1, 17-18 (1966); Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1538-39 (Fed. Cir. 1983).

8. There is no evidence that any of the secondary factors are relevant in the present case. There is no evidence of a long felt need and no evidence of commercial success to the claimed invention. (Master's Report at 31-32).

9. Obviousness under 35 U.S.C. § 103 is a question of law based on underlying fact issues. Union Carbide Corporation v. American Can Company, 724 F.2d 1567, 1573 (Fed. Cir. 1984).

10. The Allen and Westerfield and Stalcup references anticipate claims 1,

2, 6, 8, 9 and 11-14 under 35 U.S.C. § 102(b) by clear and convincing evidence and rebut the presumption of validity that attaches to a patent under 35 U.S.C. § 282. The Allen and Westerfield reference similarly anticipate claim 7. (Findings of Fact 19-45).

11. Each of claims 1 through 14 of the '635 patent are rendered obvious under 35 U.S.C. § 103 by the Allen and Westerfield and Springer references and by the Stalcup and Springer references by clear and convincing evidence, and these references rebut the presumption of validity that attaches to a patent under 35 U.S.C. § 282. (Findings of Fact 19-45).

12. The '635 patent is thus invalid in its entirety.

13. Any finding of fact determined to be a conclusion of law is so deemed, and any conclusion of law determined to be a finding of fact is so deemed.

Respectfully submitted,
SPENSLEY HORN JUBAS & LUBITZ
Martin R. Horn
John Land
David A. Hall
Dated: May 7, 1987

By John Land
Attorneys for Defendant
HITACHI AMERICA, LTD.

So Ordered: Stephen V. Wilson
U.S.D.J.
Date: October 28, 1987

Philip P. Berelson
BROWN & BAIN
600 Hansen Way, Suite 100
Palo Alto, California 94306
(415) 856-9411
Edwin H. Taylor
James C. Scheller, Jr.
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(213) 207-3800

UNITED STATES DISTRICT COURT
FOR THE CENTRAL DISTRICT OF CALIFORNIA

Civil No. 85 0262 SVW (Bx)

FINDINGS OF FACTS AND CONCLUSIONS OF LAW RE: SUMMARY JUDGMENT OF INVALIDITY OF U.S. PATENT No. 4,438,491.

Judge Stephen V. Wilson

JAMES CONSTANT,

Plaintiff,

v.

ADVANCED MICRO-DEVICES, INC., ET AL.,

Defendants.

INTRODUCTION

The Court, having considered the Motion by Intel Corporation ("Intel"), joined by Texas Instruments, Inc. for summary judgment of invalidity of U.S.

Patent No. 4,438,491 and having considered the submissions and evidence of the parties makes the following Findings of Fact and Conclusions of Law:

1. This is patent infringement suit involving inter alia, U.S. Patent No. 4,438,491 ('491) issued by the U.S. Patent and Trademark Office ("PTO") on March 20, 1984. Plaintiff James Constant, the owner and named inventor of the '491 patent has sued Intel Corporation ("Intel") and the other Defendants in this action for infringement of the '491 patent. Plaintiff originally alleged that a semiconductor "chip" manufactured by Intel, Part No. 2920, infringes the '491 patent. Plaintiff has also alleged infringement of that patent by

other chip products made by the other Defendants to this action. Defendant Intel, a California corporation, filed a motion for summary judgment under F.R.Civ.P. 56 (Intel's Motion) claiming the '491 patent is invalid since among other reasons the 2920 was on sale more than one year before the filing of the application which resulted in the '491 patent.

THE '491 PATENT

2. The application for the '491 patent was filed with the PTO on October 14, 1980; consequently, any activity prior to October 14, 1979 is more than one year prior to the date of the application for the '491 patent.

3. The '491 patent describes the interconnection of semiconductor chips which are used in computers.

4. Digital signals used in computers are binary values having two possible values, 0 and 1, which are generally represented by two different voltage levels (e.g., 0 volts and 5 volts). Several of these binary "bits" are typically used to represent a numerical value. In contrast, analog signals are represented by a continuum of voltage levels rather than discrete voltage levels associated with the 0's and 1's in a digital system. See paragraph 7 of the Declaration of Marcian E. Hoff, Jr., executed on December 12, 1985 (hereinafter referred to as "Hoff I Decl."). Thus a single analog voltage level on a single wire can represent the same number that would require several wires to represent instantaneously in digital

form.

5. Figure 1 of the '491 patent shows that in what the patent characterizes as prior art, several wires are used to connect signals between chips; for example, one wire for each bit of a digital signal. Each wire connected to a chip requires a bonding pad to which the wire is attached. These pads occupy a portion of the semiconductor chip. Therefore, several pads are needed on each of the chips to interconnect a digital signal between the chips.

6. Also, included on these chips, such as those shown in Figure 1 of the '491 patent, are logic circuits. The logic circuits, in the prior art (and in the invention), perform the manipulation of data and signals to

achieve the results desired by the designer. The logic circuits on the computer chips used in the prior art and in the claimed invention generally operate directly on digital signals. Figure I prior art, a logic circuit on one chip communicates with a logic circuit on another chip through the several wires connected between the chips; for example, a four bit digital word would be transmitted over the four wires shown in Figure I. Each wire requires a pad on each chip; therefore each chip must devote valuable area for these pads.

7. Figure 2 of the '491 patent shows an embodiment of the claimed invention where, as it can be seen, the number of wires between the chips has been reduced to a single wire. Some of

the pads on each chip have been eliminated and replaced with a transmitter - receiver ("transceiver") which is connected between a pad and the logic circuits. A single wire links the pads between two chips to permit the logic circuits on each of the chips to communicate.

8. The '491 patent gives a number of examples for transceivers. For example, the '491 patent notes that a transmitter may be a digital-to-analog (D/A) converter and the receiver may be an analog-to-digital (A/D) converter.

9. An analog-to-digital ("A/D") converter is an electrical circuit that converts an analog signal to a digital signal. Hoff I Decl. para. 7.

10. A digital-to-analog ("D/A") converter is also an electrical

circuit, but it performs the opposite function. It converts a multi-line digital signal to a single-line analog signal. For example, 8 bits (on eight wires or lines) each representing a "1" or a "0" are converted to an analog signal on a single wire or line. Declaration of Marcian E. Hoff, Jr. (HOFF III DECL.) filed November 15, 1986, para. 5.

11. In Figure 2 of the '491 patent, the output from the logic circuit on chip 1 is connected to the transceiver 15 which, in one embodiment, includes a D/A converter which acts as a transmitter by converting the digital signals to an analog signal. The analog signal is carried to the pad 11 and then over the single line 31 to pad 21 on chip 2.

Pad 21 is connected to a receiver, specifically an A/D converter 25 which reconverts the analog signal to digital signals for use by the logic circuit on chip 2.

12. The goal of the '491 patent is "to reduce the on-chip area devoted to interface and to reduce the number of wires needed for interconnecting chips of a computer. The method of the invention is equally simple, namely, the steps of including at least one of a transmitter and receiver means in a monolithic IC chip and interconnecting chips to form a computer." (col. 6, line 50 to col. 7, line 3, '491 patent). The foregoing concept is claimed in varying embodiments in the 30 claims of the '491 patent; these embodiments vary in terms of the

particular transceiver used.

13. It is undisputed that the numerous transceiver examples described in and appearing in the claims of the '491 patent, such as modems, shift registers, A/D converters, codecs, etc. were well-known elements when the application for the '491 patent was filed. The '491 patent states that the choice of the transceivers is "a standard communication task." Col. 4, 1-11, '491 patent.

14. The 2920 is a digital microcomputer chip developed and manufactured by Intel. The development of the 2920 began in late 1975 and culminated in 1979 with the introduction of this part, after testing of the part during March 1979. (Hoff I, Decl., para. 6). Photographs

of the 2920 chip were published during March 1979. See Hoff I Decl. Exhibit 3.

15. There are several articles describing the 2920 which were published more than one year before the filing date of the '491 patent (Hoff I Decl. Exhibits 2-9).

16. Intel offered the 2920 for sale no later than September 1979 and fulfilled an order from General Electric for a 2920 in September of 1979. (Decls. of Elmer Cougle, Dennis Lundien, and Donald Ellers, all filed December 18, 1985.)

17. Plaintiff admitted that the Intel 2920 was sold as early as September 1979 and that "Intel first started advertising the 2920 for sale in September, 1979." (Paragraph 11 of

Decl. of Plaintiff James Constant executed 13 April, 1987.)

18. Initially, Intel's Motion relied substantially on its September 1979 sale as the basis for invalidity under 35 USC 102(b). Texas Instruments, another defendant, joined on the motion. Plaintiff opposed Intel's motion by asserting that the 2920 chip itself did not come within the claims, but only because the single chip which was placed on sale lacked the preamble of the claims of the '491 patent, that is, it was not in a computer, etc. Intel than filed additional motion papers relying on the 2920-related publication and the Field patent.

19. Plaintiff's first letter to Defendant Intel charging infringement

advised Intel that the 2920 chip infringed the '491 patent: "Your 2920 Signal Processor infringes Claims 1, 7, 8, 9, 16, 18 and 23, as minimum, of my enclosed patent... In these circumstances, you will have to stop making, using and selling A/D and D/A units in 2920 or take a licence under my patent." Also, in the original complaint and first amended and second amended complaints, Plaintiff alleged that the 2920 chip infringed the '491 patent.

THE UNCONTROVERTED EVIDENCE ESTABLISHES THE INVALIDITY OF THE 491 PATENT

20. Intel has shown that the 2920 has all the elements of Claims 1, 7, 8, 9, 16, 18, 21, 22 and 23 (except the preamble). Plaintiff agrees with this in general although without setting

forth the specific claims. Plaintiff states that this is not sufficient for anticipation since the sale of the 2920 did not fulfill the preamble of the claims (e.g., the chip was not sold interconnected to other chips in a computer). Intel has argued that this preamble need not be shown and that therefore the sale of the 2920 alone invalidates the '491 patent. This Court, for purposes of this motion, assumes that Plaintiff is correct in requiring a showing that the conditions of the preamble have been met. Therefore, the Court has examined the publications for the preamble of the claims as well as all other elements of the claims.

21. Hoff I Decl. Exhibit 5 is a printed publication which was made

publicly available by Intel beginning in September 1979. (Decl. of Sherrie Zirkle filed April 9, 1987.) Plaintiff has stated that this publication should not be considered because it was stamped "Advanced Information." The Court disagrees with Plaintiff. The document was publicly available, without restriction.

22. Hoff I. Decl. Exhibit 5 discloses the subject matter claimed in Claims 1, 7, 8, 9, 16, 18, 21, 22, and 23 including the preamble. For example, Hoff I Decl. Exhibit 5 describes the cascading of multiple 2920s where the output of one 2920 chip is connected to the input of a second 2920 chip and so on with further 2920s if desired. A normal and intended use of 2920s in such a cascade would be to

communicate between the chips with analog signals which are converted into digital signals for internal processing in the micro computers within the 2920 chips. A reduction of interconnections inherently occurs in such an arrangement. Moreover, Plaintiff admits Exhibit 5 of Hoff I Decl. teaches computer applications of the 2920. See Plaintiff's Presentation '491 Patent (dated October 29, 1986), pages 3 and 4.

23. The 2920 is a more complex chip than that shown in Figure 2 of the '491 patent. It can, for example, receive up to four analog signals and change one or more of them to digital signals, Likewise, it can output more than one analog signal. The use of a single analog signal into and from the

2920 is a subset of the 2920's total capability; this single input and output use is clearly shown in Figure 1 of Exhibit 9. Therefore, the cascading of the chips in its simplest form provides what is shown in Figure 3 of the '491 patent (compare Figures 2 and 3 of '491 patent with Exhibits 5 and 9).

24. It is possible to program the 2920 for applications where there is no reduction of interconnections. This does not change the fact that the uses described above automatically reduces interconnections, and such reductions are inherent in the descriptions of applications for the 2920 in Hoff I Decl. Exhibit 5.

25. Hoff I Decl. Exhibit 9 is a printed publication which was

distributed publicly as part of a magazine in September 1979. (Decls. of Kimberly Douglas and Lori Shulman, filed April 9, 1987.)

26. Hoff I Decl. Exhibit 9 describes the 2920 chip and several applications for this chip, including a signal processing application.

30. The record shows by clear and convincing evidence that the 2920 chip, and uses for that chip, were widely publicized by Intel more than one year before the filing of the '491 patent application in various printed publications including Hoff I Decl. Exhibit 9.

31. Applications intended and described for the 2920 in these printed publications prior to October 1979 include multi-chip applications

involving computers in which the interconnections between chips is reduced because of the use of the A/D and D/A converters on the 2920. The various block diagram illustrations of the 2920 shown in Hoff I Decl. Exhibits 3, 5 and 9 indicate that a reduction of interconnections will take place when an analog signal is converted to a digital signal and than processed by the 2920.

32. Mr. Constant has, after Mr. Hillman's Report on the '491 patent, asserted that the publications do not anticipate because they do not show a specific computer program. The claims of the '491 patent relate to a set of physical ("hardware") components. The claims do not require a computer program. The specification of the '491

patent, in accordance with the claims of the patent, does not disclose any specific computer program nor does it suggest that a computer program is a part of the invention.

33. The persons working in the field to which the '491 patent belongs during the period 1977-1979 were highly skilled. Dr. Hoff of Intel had a PhD in engineering and many years of experience in electrical engineering. He headed up Intel's development of the 2910 and 2920. Plaintiff contends that a person of ordinary skill in the art is a "DSP (digital signal processing) designer, user, teacher or author who has considerable experience ... in dealing with interconnecting DSP chips." (Plaintiff's Objections to Master's Report, Part 1, dated February

17, 1987, page 7.) Also Plaintiff states persons working in the field of the related patent in suit (3,950,635) have at least one college degree in engineering or physics (Deposition of Constant, Pages 115-119, Vol. 1, March 20, 1986). Therefore, one of ordinary skill in the art during the pertinent period had a degree in science, experience in electrical engineering and some experience in digital signal processing chips.

34. Certain claims of the '491 patent (i.e., Claims 2-6, 10-15, 17, 19-20 and 24-30) are not completely described in Intel's Exhibits 5 or 9 of Hoff I Decl. These claims ("Remaining Claims") relate to the use of certain equivalent structures which are substituted in place of the transmitter

or receiver, such as the A/D or D/A converter. Plaintiff James Constant concedes in the '491 patent that these equivalent transmitter and receivers are conventional communication system elements which may be implemented by one with ordinary skill in the art. See, e.g., Column 3, lines 60-66 of the '491 patent; column 4, lines 11-13 of the '491 patent; and Plaintiff's Amendment submitted to the U.S. Patent Office which Amendment is dated August 26, 1983. (See, e.g., pages 12-13 of that Amendment: "In view of the foregoing references for placing LEDs and photodetectors on chips (Moulton, Fang), for use of acoustic wave connections (U.S. Patent 4,035,775), for placing optical means on a chip and using fiber interconnections (Math,

Moulton, Gadzinsky, Fang), for placing microwave means on chips and using microwave cable interconnections (Sobol), for placing A/D and D/A converters on a chip (Runyon), for placing logic circuits and interfacing means on a chip (Scientific American), for placing modems and codecs on a chip (Young, Pastorino, Mayo in Scientific American, Miller, Hoff), the placing of samplers and multiplexers on chips (Mayo in Scientific American, Hoff, Faggian), and the connection of logic circuits to communications interfaces on a chip (Sutherland and Mead in Scientific American, page 211), the placing and connection of applicant's logic circuits and transceivers on the same chip can be made without undue experimentation by the routineer.")

These statements in the file wrapper of the '491 patent reflect upon the ordinary skill in the art and define generally the art and the skill of the art.

35. The differences between the subject matter of the "Remaining Claims" are simply the substitution of Hoff I. Decl. Exhibit 5 with various types of well-known transmitters and receivers.

36. Exhibits 3, 5, and 9 of Hoff I Decl. taken together render the subject matter of the Remaining claims obvious to one with ordinary skill in the art. There is no evidence of any secondary factors that weigh against obviousness.

CONCLUSIONS OF LAW

1. Conclusions 1-9 set forth

above in connection with the '635 patent are incorporated herein by reference.

2. Summary judgment is appropriate when there is no genuine issue of material fact and the movant is entitled to judgment as a matter of law. See, e.g., SRI International v. Matsushita Electric Corp. of America, 775 F.2d 1107, 1116 (Fed. Cir. 1985); Chore-Time Equipment, Inc. v. Cumberland Corp., 713 F.2d 774, 778 (Fed. Cir. 1983). The moving party bears the burden of demonstrating an absence of all genuine issues of material fact. Cooper v. Ford Motor Co., 748 F.2d 677, 679 (Fed. Cir. 1984). However, where the evidence on an issue leaves no room for any reasonable difference of opinion as to

its resolution, the District Court should resolve such issue as a matter of law. Jamesbury Corp. v. Litton Industrial Products, Inc., 756 F.2d 1556, 1560 (Fed. Cir. 1985). Indeed, once a prima facie case for summary judgment exists, the party opposing the motion must point to a material evidentiary conflict created on the record. And mere denials or conclusory statements are insufficient. Barmag Barmer Maschinenefabrik AG v. Murata Machinery Co., Ltd., 731 F.2d 831 (Fed. Cir. 1984).

3. A printed publication which describes a patented invention anticipates that patented invention if the printed publication was published more than one year before the filing of the application resulting in the

patent. 35 USC 102(b).

4. A printed publication exists for purposes of Section 102(b) if even a limited number of copies of the publication were publicly available to those in the art seeking to obtain the publication. Hamilton Laboratories v,. Massengill, 111 F.2d 584 (6th Cir. 1940), cert. den. 311 U.S. 688.

5. Hoff I Decl. Exhibits 3, 5 and 9 are printed publications under 35 USC 102(b) which anticipate Claims 1, 7, 8, 9, 16, 18, 21, 22, and 23 of the '491 patent, rendering those claims invalid.

7. The 2920 chip, for purposes for USC 102(b), was placed on sale by Defendant Intel more than one year before the filing date of the '491 patent. Thus, tne 2920 chip is in the prior art with respect to the '491

patent.

8. Hoff I Decl. Exhibit 5 inherently discloses the inventions in Claims 1, 7, 8, 9, 16, 18, 21, 22, and 23 of the '491 patent. Printed publications which inherently disclose an invention anticipate the invention. Tyler Refrigeration v. Kysor Industrial Corp., 777 F.2d 687 (Fed. Cir. 1985).

9. A reference does not anticipate an invention if the reference achieves an anticipation that was unintended and unappreciated and was not a necessary consequence of the use of the object in the prior art. Tilghman v. Proctor, 102 U.S. 707, 26L. Ed. 279 (1881). Intel's references anticipate because the reduction of interconnections using the 2920 are intended consequences of the placement

of the transmitter and receiver on the chip and the reduction of interconnections occurs as a necessary consequence of intended and described uses.

9. Claims 11, 7, 8, 9, 16, 18, 21, 22 and 23 of the '491 patent are thus invalid for anticipation by Hoff I Decl. Exhibit 5, under 35 USC 102(b).

10. The Remaining Claims of the '491 patent are invalid for obviousness under 35 USC 103. Application of Borcherdt, 197 F.2d 550 (CCPA 1952); Application of Stewart, 222 F.2d 747 (CCPA 1955).

11. All of the claims of the '491 patent are invalid as to all Defendants in this action and therefore, all allegations of infringement of the '491 patent against all Defendants are

dismissed with prejudice.

Dated:October 28, 1987

Judge Stephen V. Wilson

Presented by:

BROWN & BAIN
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Edwin H. Taylor
an Attorney for Defendant,
INTEL CORPORATION

Dated: 5/19/87

RICHARD D. FYBEL
ADRIAN M. PRUETZ
MORRISON & FOERSTER
333 South Grand Avenue, Suite 3800
Los Angeles, California 90071
Telephone: (213) 626-3800

Attorneys for Defendant
FUJITSU MICROELECTRONICS, INC.

SUBMITTED ON BEHALF OF ALL DEFENDANTS

UNITED STATES DISTRICT COURT
FOR THE CENTRAL DISTRICT OF CALIFORNIA
No. 85 0262 SVW (Bx)
ORDER GRANTING DEFENDANTS' MOTION TO RETAX COSTS AND DENYING PLAINTIFF'S MOTION TO DISMISS AND DISALLOW COSTS AND FOR SANCTIONS

DATE: May 2, 1988
TIME: 1:30 p.m.
PLACE: Courtroom F

JAMES CONSTANT
Plaintiff,

v.

ADVANCED MICRO-DEVICES, INC., at al.,
Defendants.

Defendants' motion to retax certain costs and plaintiff's motion to dismiss determination of costs, disallow costs and for sanctions against defendants came on for hearing before the United States District Court, Honorable Stephen V. Wilson presiding, on May 2, 1988 at 1:30 p.m., upon due notice. Defendant Fujitsu Microelectronics, Inc. ("FMI") appeared through its counsel, Adrian M. Pruetz of Morrison & Foerster, and FMI represented the position of all defendants in the matter. Plaintiff James Constant appeared in his own behalf. The Court, having reviewed the memoranda, evidence and legal authorities filed in support of and in opposition to defendants' motion to retax certain costs and plaintiff's

motion to dismiss and disallow costs and for sanctions, and having heard the arguments presented at the hearing;

IT IS HEREBY ORDERED:

1. Plaintiff's request that this Court recuse itself is DENIED.

2. Defendants' motion to retax the costs of the Special Master Robert Hillman and the costs of reproduction of specified documents against plaintiff is GRANTED, and plaintiff is ordered to pay defendants' costs for those items in the amount of $95,289.71.

3. Plaintiff's motion to dismiss determination of costs, to disallow costs and for sanctions is DENIED, the costs taxed by the Clerk of Court in the Bill of Costs are affirmed, and plaintiff is ordered to pay defendants

costs for those specified items in the amount of $28,542.29.

4. In accordance with the foregoing orders, costs in the total amount of $123,832.00 shall be entered into and made part of the Judgment entered in favor of defendants and against plaintiff on November 9, 1987, such costs to bear interest at the legal rate from date of entry, and such costs when recovered shall be payable to each defendant in the amount allowed.

DATED: May 10, 1988

Honorable Stephen V. Wilson
United States District Judge

CERTIFICATE OF SERVICE

I certify that the foregoing

APPENDIX B

was served on all parties on

17 August, 1988

by mailing first class a true and correct copy thereof to them addressed as follows:

cc: Counsel for Advanced Micro-Devices, Inc. and Intel Corporation

Edwin Taylor
Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Blvd., 7th Fl.
West Los Angeles, CA 90025

Counsel for Gould, Inc. and American Microsystems, Inc.

Joseph Golant
Romney, Golant, Marten & Ashen
10920 Wilshire Blvd.
Suite 1000
Los Angeles, CA 90024

Counsel for Analog Devices, Inc. and NEC Electronics, Inc.

Robert Schroeder
Pretty, Schroeder, Brueggeman & Clark
444 South Flower Street, Suite 2000
Los Angeles, CA 90071

Counsel for Fujitsu Microelectronics, Inc.

Richard Fybel
Morrison & Foerster
333 South Grand Avenue
38th Fl.
Los Angeles, CA 90071

Counsel for Digital Switch, Inc. and
Granger Associates, Inc.

Howard Brody
Grossman, Graven, Perry & Block
523 West Sixth Street, Suite 1130
Los Angeles, CA 90014-1109

Counsel for Hitachi America, Ltd.

Martin Horn
Spensley, Horn, Jubas & Lubitz
188 Century Park East, 5th Fl.
Los Angeles, CA 90067

Counsel for Paradyne Corp.

Kristin Cano
Curtis & Vaccaro
Manufacturers Bank Bldg.
One Newport Place, Suite 700
Newport Beach, CA 92660

Counsel for Texas Instruments, Inc.

Paul Malingagio
Sheppard, Mullin, Richter & Hampton
333 South Hope Street, 48th Fl.
Los Angeles, CA 90071

Counsel for Rockwell International Corp. and TRW, Inc.

Allen Katz
Munger, Tolles & Rickershauser
612 South Flower Street, 5th Fl.
Los Angeles, CA 90017

Solicitor General
Department of Justice
Washington, D.C. 20530

Date: 17 August 1988

James Constant
1603 Danbury Dr
Claremont, CA 91711
(714) 624-1801

pro se petitioner